LISTING OF THE CLAIMS:

A listing of the claims is presented below:

1. (Previously Presented) A method of improving reliability of a semiconductor device comprising at least one layer of low-K ILD, steps of which comprise:

providing a semiconductor device comprising:

a semiconductor chip comprising copper electrical interconnections and at least one layer of low-K ILD therewithin and metallization on a surface thereof; and

a carrier substrate having electrical contact pads on a surface thereof to which the semiconductor chip is electrically interconnected through an electrically conductive material to the copper electrical interconnections; and

optionally, a second semiconductor chip having opposed surfaces, one of which for bonding to the carrier substrate and the other of which for establishing electrical interconnection with both the semiconductor chip and the carrier substrate, wherein the carrier substrate has electrical contact pads on a surface thereof to which at least one of the semiconductor chip or the second semiconductor chip is electrically interconnected;

providing a heat curable composition either between the electrically interconnected surfaces of the semiconductor chip and the carrier substrate to form a semiconductor device assembly and/or over the semiconductor; and

exposing the semiconductor device assembly to elevated temperature conditions sufficient to cure the heat curable composition,

wherein the heat curable composition comprises a curable resin component and a filler component, wherein the filler component is present in an amount sufficient to provide the heat curable composition when cured with a coefficient of thermal expansion of less than about 25 ppm/°C or a coefficient of thermal expansion of greater than about 50 ppm/°C and when cured the heat curable composition has a ratio of modulus versus temperature between -65°C and 125°C in the range of 10MPa/°C to about -10MPa/°C.

Claims 2-4. (Cancelled)

5. (Original) The method of Claim 1, wherein the electrically conductive material is solder.

6. (Original) The method of Claim 5, wherein the solder is selected from the group consisting of Sn(63):Pb(37), Pb(95):Sn(5), Sn:Ag(3.5):Cu(0.5) and Sn:Ag(3.3):Cu(0.7).

7. (Previously Presented) An underfilled semiconductor device assembly comprising:

Either a semiconductor chip comprising copper electrical interconnection and the layer of low-K ILD therewithin and metallization on a surface thereof or a semiconductor device comprising a semiconductor chip comprising copper electrical interconnection thereof contacting at least one layer of low-K ILD therewithin and metallization on a surface thereof to which is electrically connected a carrier substrate;

a circuit board having electrical contact pads on a surface thereof to which the semiconductor chip or semiconductor device, respectively, is electrically interconnected; and

a heat curable underfill composition between the semiconductor chip or semiconductor device, respectively, and the circuit board,

wherein the heat curable underfill composition comprises a curable resin component and a filler component, wherein the

filler component is present in an amount sufficient to provide the heat curable underfill composition when cured with a coefficient of thermal expansion of less than about 25 ppm/°C or a coefficient of thermal expansion of greater than about 50 ppc/°C, and wherein the heat curable underfill composition has a ratio of modulus versus temperature between -65°C and 125°C in the range of -10MPa/°C to about 10MPa/°C.

8. (Previously Presented) The device of Claim 7, wherein the electrically conductive material is solder.

9. (Original) The method of Claim 8, wherein the solder is selected from the group consisting of Sn(63):Pb(37), Pb(95):Sn(5), Sn:Ag(3.5):Cu(0.5) and Sn:Ag(3.3):Cu(0.7).

Claims 10-22. (Cancelled)

23. (Original) A method of assembling a semiconductor device with improved reliability, steps of which comprise:

providing a semiconductor chip having opposed surfaces, one of which for bonding to a carrier substrate and the other of which having electrical interconnections for establishing electrical interconnection therewith, and having a thickness of less than 100 microns;

providing a carrier substrate having a portion of a surface for bonding the semiconductor chip and another portion of a surface for establishing electrical interconnection with the semiconductor chip;

providing a heat curable die attach composition onto at least a portion of one or both of the bonding surface of the semiconductor chip or the bonding surface of the carrier substrate, in an amount sufficient to establish a bondline of less than about 10 microns when the semiconductor chip and the carrier substrate are mated;

mating the bonding surface of the semiconductor chip with the bonding surface of the carrier substrate to form a semiconductor device assembly and exposing the semiconductor device assembly to elevated temperature conditions sufficient to cure the heat curable die attach composition, thereby bonding the semiconductor device to the carrier substrate; and

establishing electrical interconnections between the semiconductor device and the carrier substrate,

wherein when cured the heat curable die attach composition has a ratio of modulus versus temperature between -65°C and 125°C in the range of -10MPa/°C to about -10MPa/°C.

24. (Original) The method of Claim 23, wherein the heat curable die attach composition comprises a curable resin component and a filler component, wherein the filler component is present in an amount sufficient to provide the heat curable die attach composition when cured with a coefficient of thermal expansion of less than about 25 ppm/°C or a coefficient of thermal expansion of greater than about 50 ppm/°C.

25. (Original) A semiconductor device comprising:

a semiconductor chip having opposed surfaces, one of which for bonding to a carrier substrate and the other of which having electrical interconnections for establishing electrical interconnection therewith, and having a thickness of less than 100 microns;

a carrier substrate having a portion of a surface for bonding the semiconductor chip and another portion of a surface for establishing electrical interconnection with the semiconductor chip; and

a die attach composition between the bonding surfaces of the semiconductor chip and the carrier substrate, to form a bond line of less than about 10 microns,

wherein the die attach composition has a ratio of modulus versus temperature between -65°C and 125°C in the range of -10MPa/°C to about 10MPa/°C.